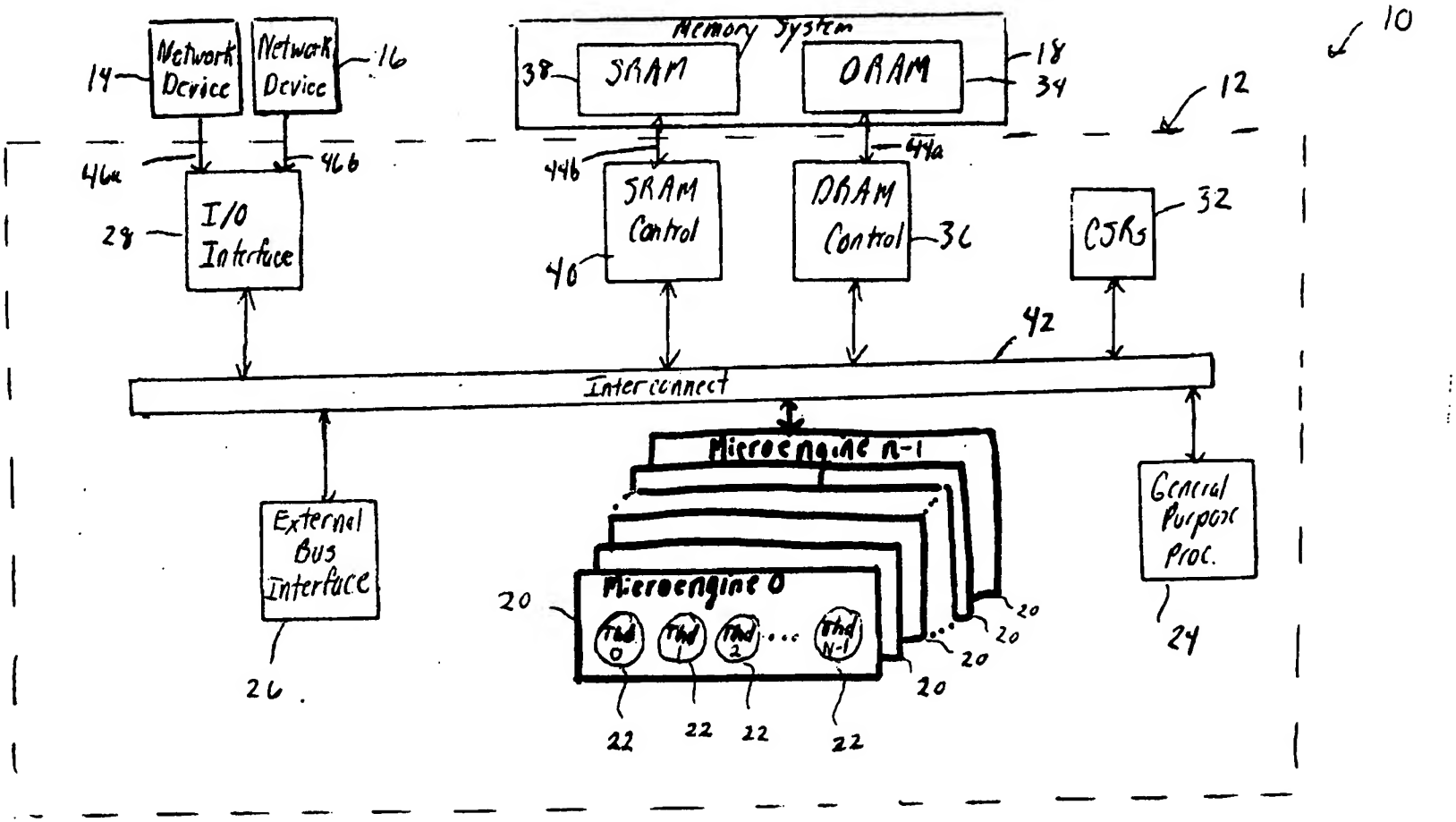
10
12
Network Device
Network Device
14
16
Memory System
SRAM
DRAM
38
18
34
46a
46b
44b
44a
I/O Interface
28
SRAM Control
DRAM Control
36
40
CSRs
32
42
Interconnect
External Bus Interface
26
Microengine n-1
Microengine 0
20
Thd 0
Thd 1
Thd 2
Thd N-1
22
General Purpose Proc.
24

FIG. 1

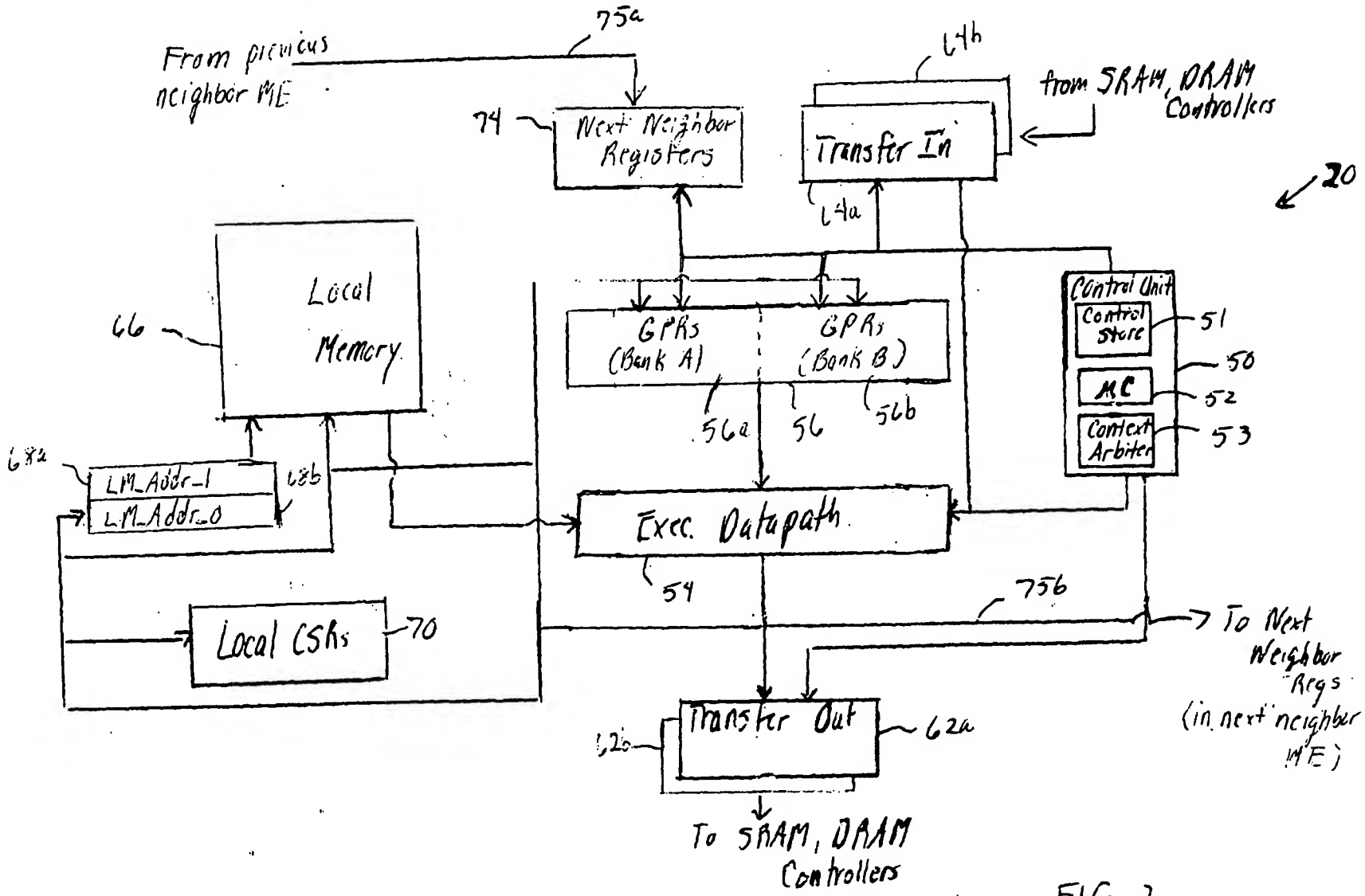
From previous neighbor ME
75a
74
Next Neighbor Registers
64b
Transfer In
from SRAM, DRAM Controllers
20
64a
Local Memory
66
GPRs (Bank A)
GPRs (Bank B)
56a
56
56b
Control Unit
Control Store
51
50
MC
52
Context Arbiter
53
68a
LM_Addr_1
LM_Addr_0
68b
Exec. Datapath
54
Local CSRs
70
75b
To Next Neighbor Regs (in next neighbor ME)
Transfer Out
62a
62b
To SRAM, DRAM Controllers

FIG. 2

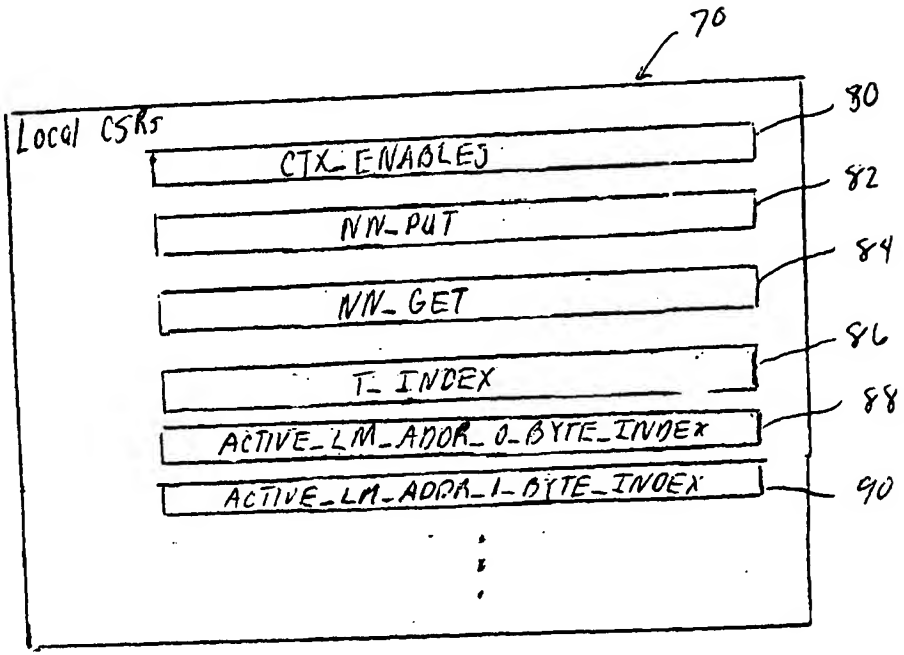
70
Local CSRs
CTX_ENABLES
80
NN_PUT
82
NN_GET
84
T_INDEX
86
ACTIVE_LM_ADDR_0_BYTE_INDEX
88
ACTIVE_LM_ADDR_1_BYTE_INDEX
90

FIG. 3

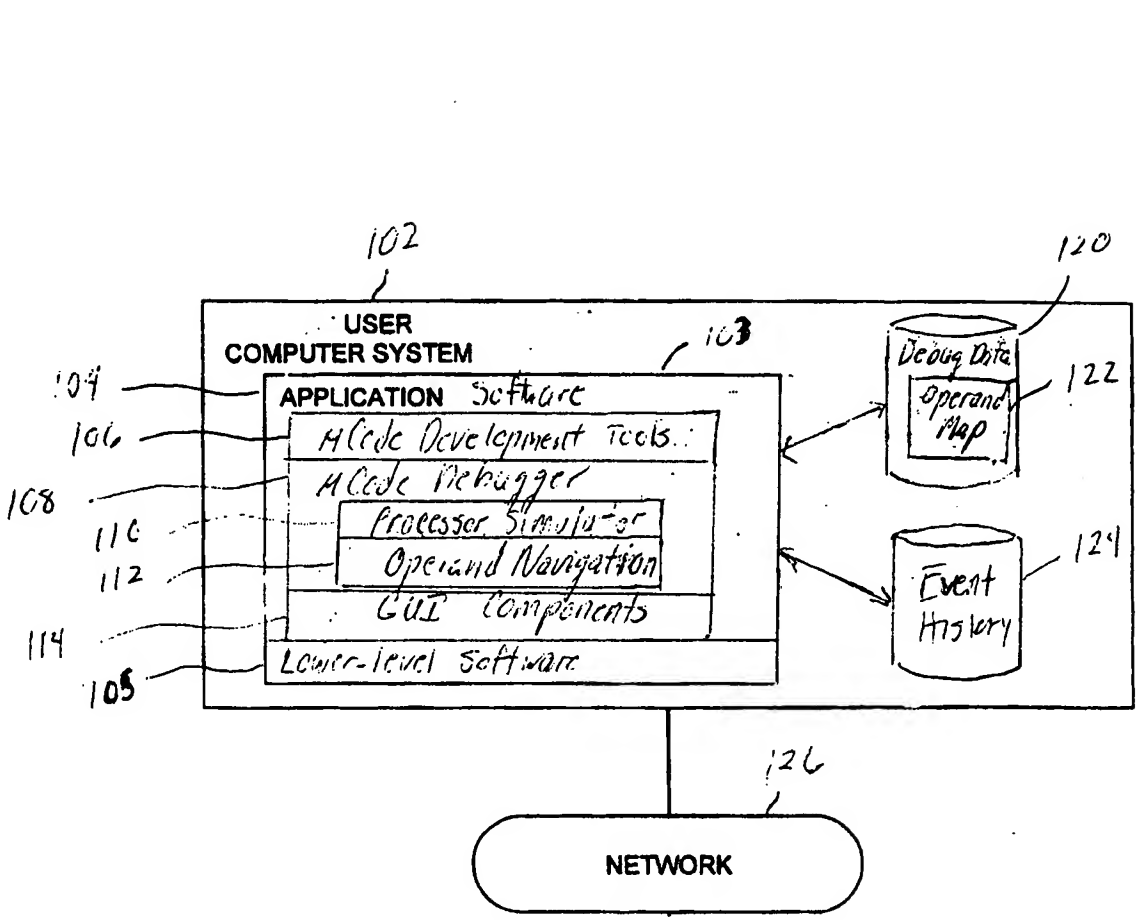
100
102
USER
COMPUTER SYSTEM
103
104
APPLICATION Software
106
MCode Development Tools
MCode Debugger
108
Processor Simulator
110
Operand Navigation
112
GUI Components
114
Lower-level Software
105
120
Debug Data
Operand Map
122
Event History
124
126
NETWORK

FIG. 4

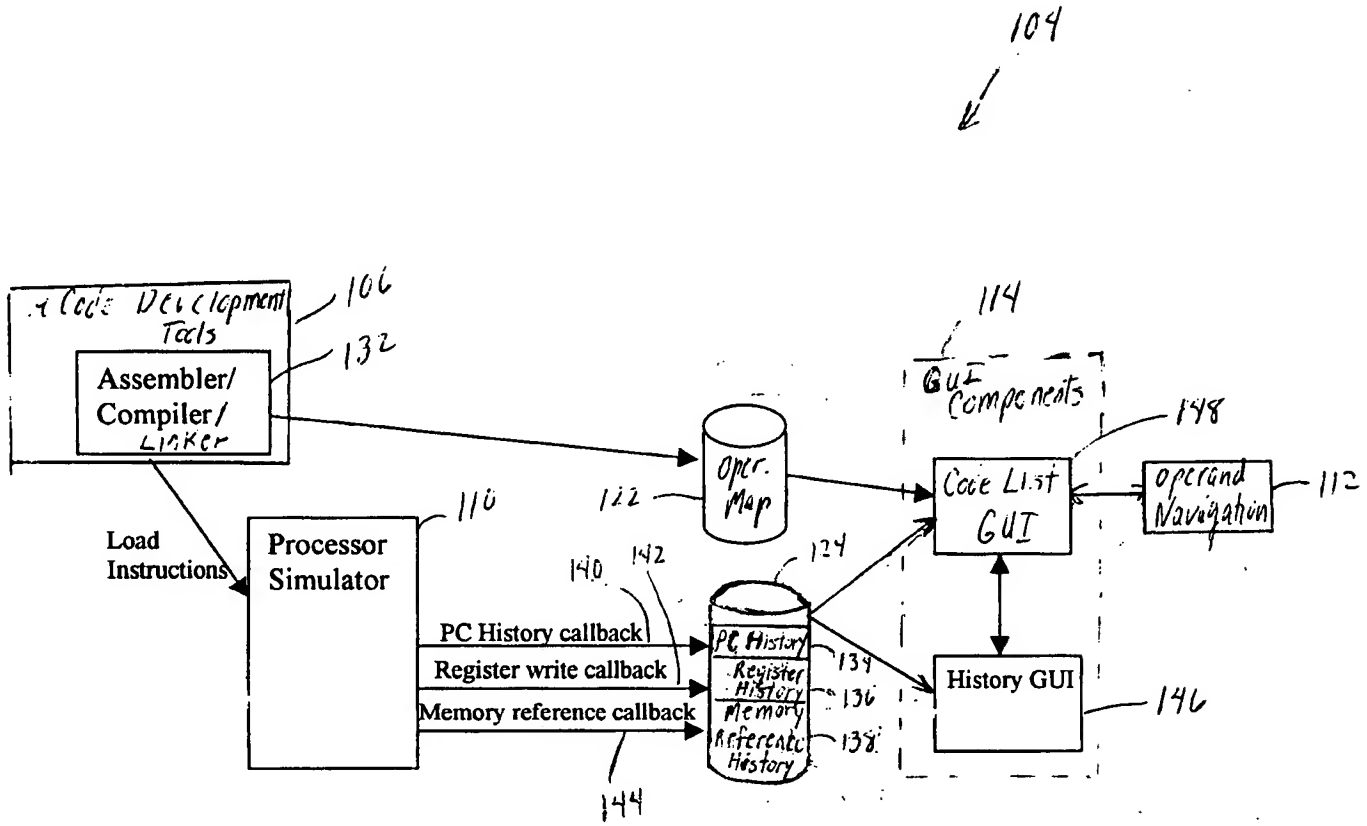
104
Code Development Tools
106
Assembler/ Compiler/ Linker
132
Load Instructions
Processor Simulator
110
Oper. Map
122
114
GUI Components
148
Code List GUI
Operand Navigation
112
140
142
124
PC History callback
Register write callback
Memory reference callback
PC History
Register History
Memory Reference History
134
136
138
History GUI
146
144

FIG. 5

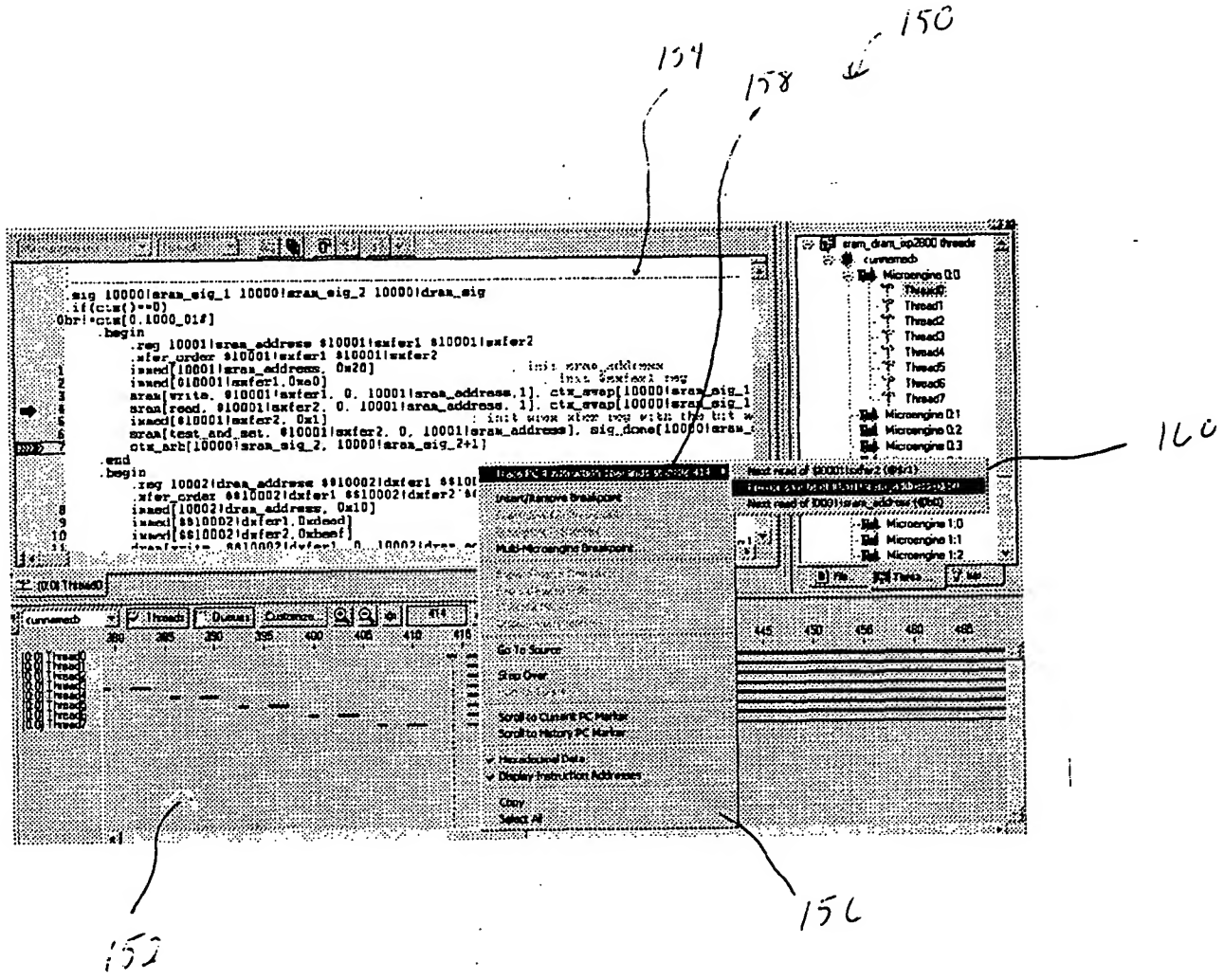

FIG. 6

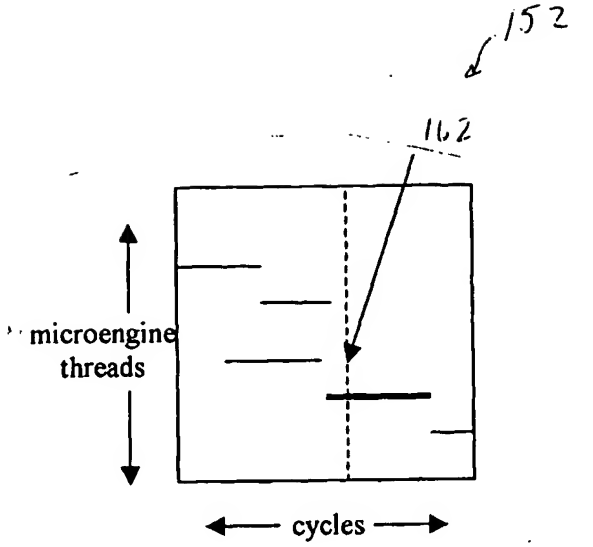
152
162
microengine threads
cycles

FIG. 7

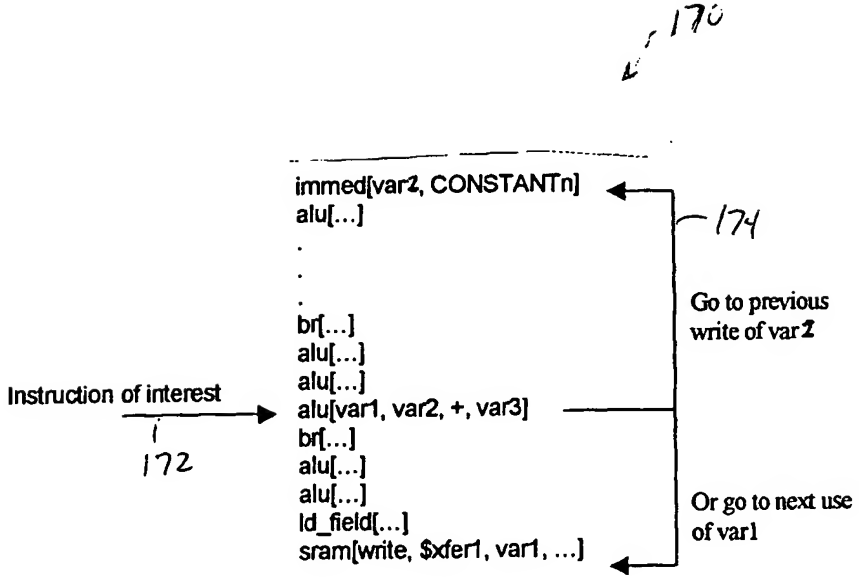
170
immed[var2, CONSTANTn]
alu[...]
.
.
.
br[...]
alu[...]
alu[...]
Instruction of interest
alu[var1, var2, +, var3]
br[...]
alu[...]
alu[...]
ld_field[...]
sram[write, $xfer1, var1, ...]
172
174
Go to previous write of var2
Or go to next use of var1

FIG. 8

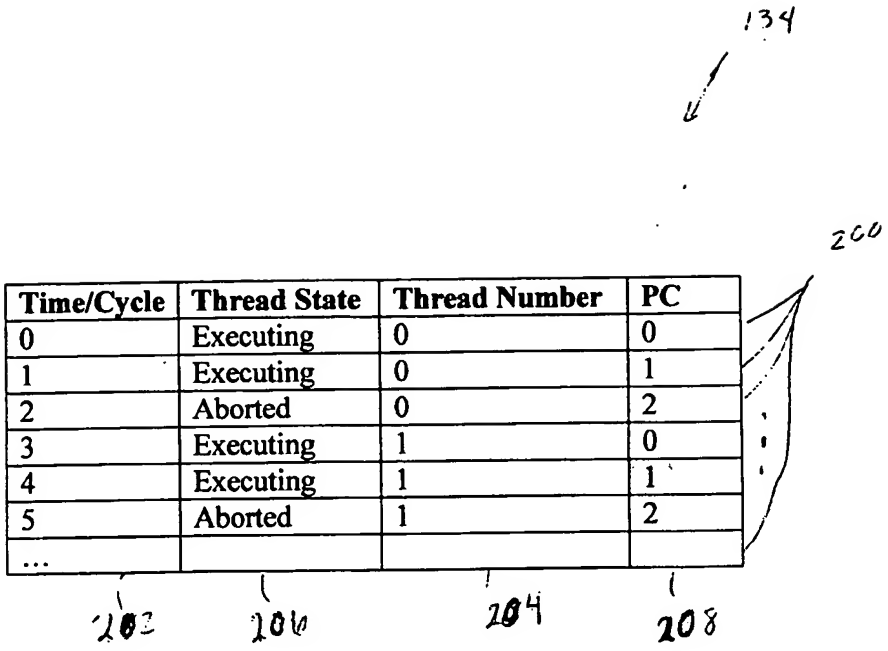
134
200
Time/Cycle
Thread State
Thread Number
PC
0
Executing
0
0
1
Executing
0
1
2
Aborted
0
2
3
Executing
1
0
4
Executing
1
1
5
Aborted
1
2
...
202
206
204
208

FIG. 10

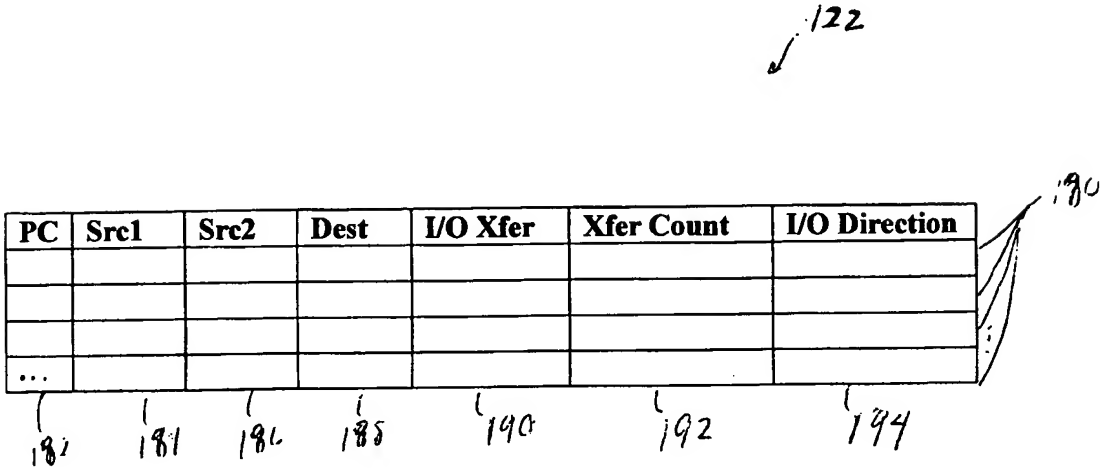
122
190
PC
Src1
Src2
Dest
I/O Xfer
Xfer Count
I/O Direction
...
182
181
186
188
190
192
194

FIG. 9

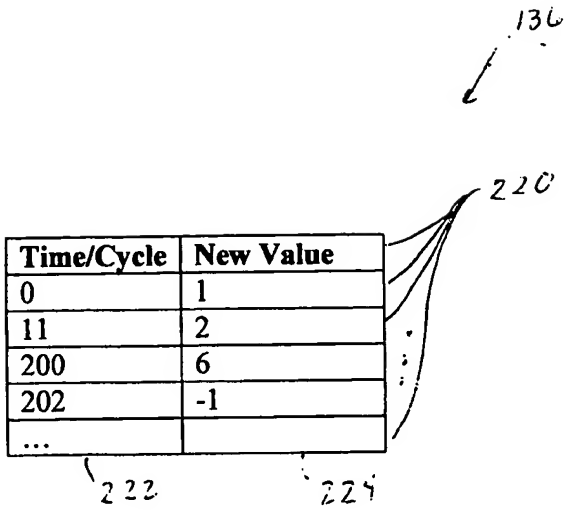
136
220
Time/Cycle
New Value
0
1
11
2
200
6
202
-1
...
222
224

FIG. 11

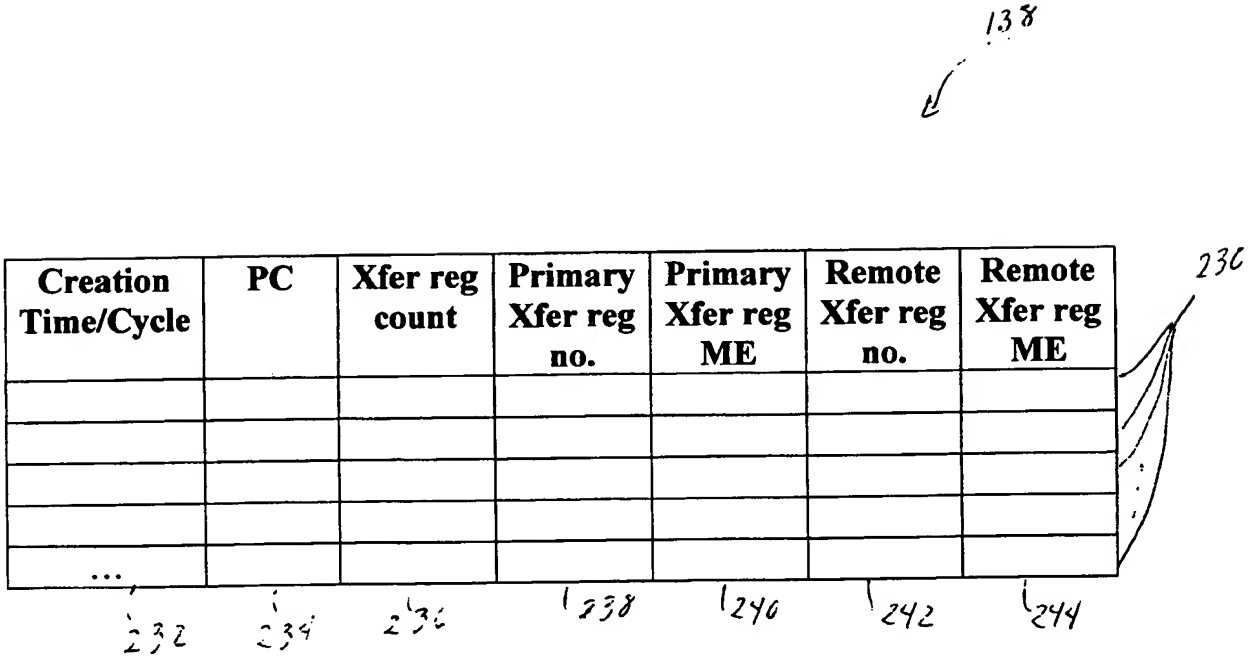
138
230
Creation Time/Cycle
PC
Xfer reg count
Primary Xfer reg no.
Primary Xfer reg ME
Remote Xfer reg no.
Remote Xfer reg ME
...
232
234
236
238
240
242
244

FIG. 12

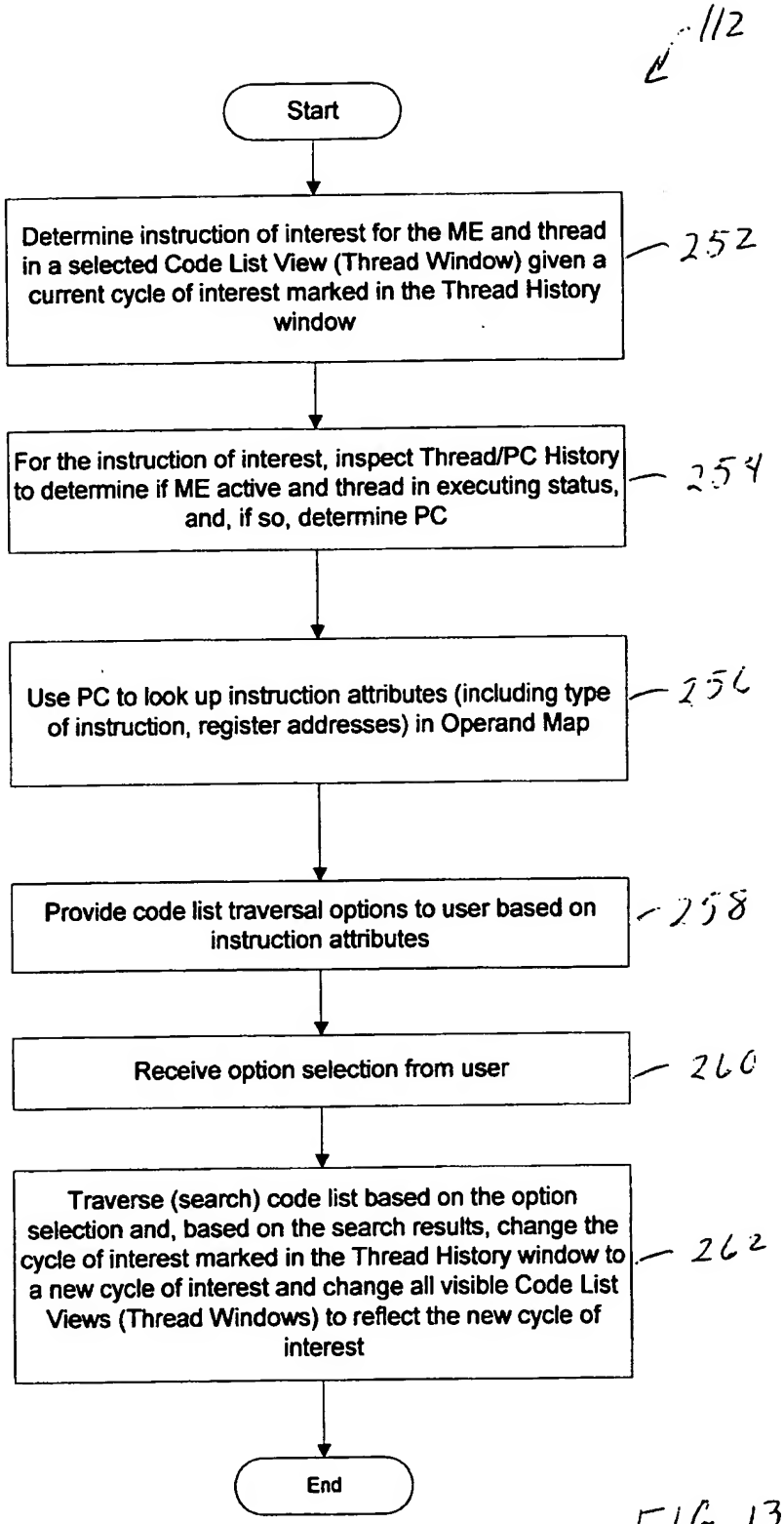
112
Start
Determine instruction of interest for the ME and thread in a selected Code List View (Thread Window) given a current cycle of interest marked in the Thread History window
252
For the instruction of interest, inspect Thread/PC History to determine if ME active and thread in executing status, and, if so, determine PC
254
Use PC to look up instruction attributes (including type of instruction, register addresses) in Operand Map
256
Provide code list traversal options to user based on instruction attributes
258
Receive option selection from user
260
Traverse (search) code list based on the option selection and, based on the search results, change the cycle of interest marked in the Thread History window to a new cycle of interest and change all visible Code List Views (Thread Windows) to reflect the new cycle of interest
262
End

FIG. 13

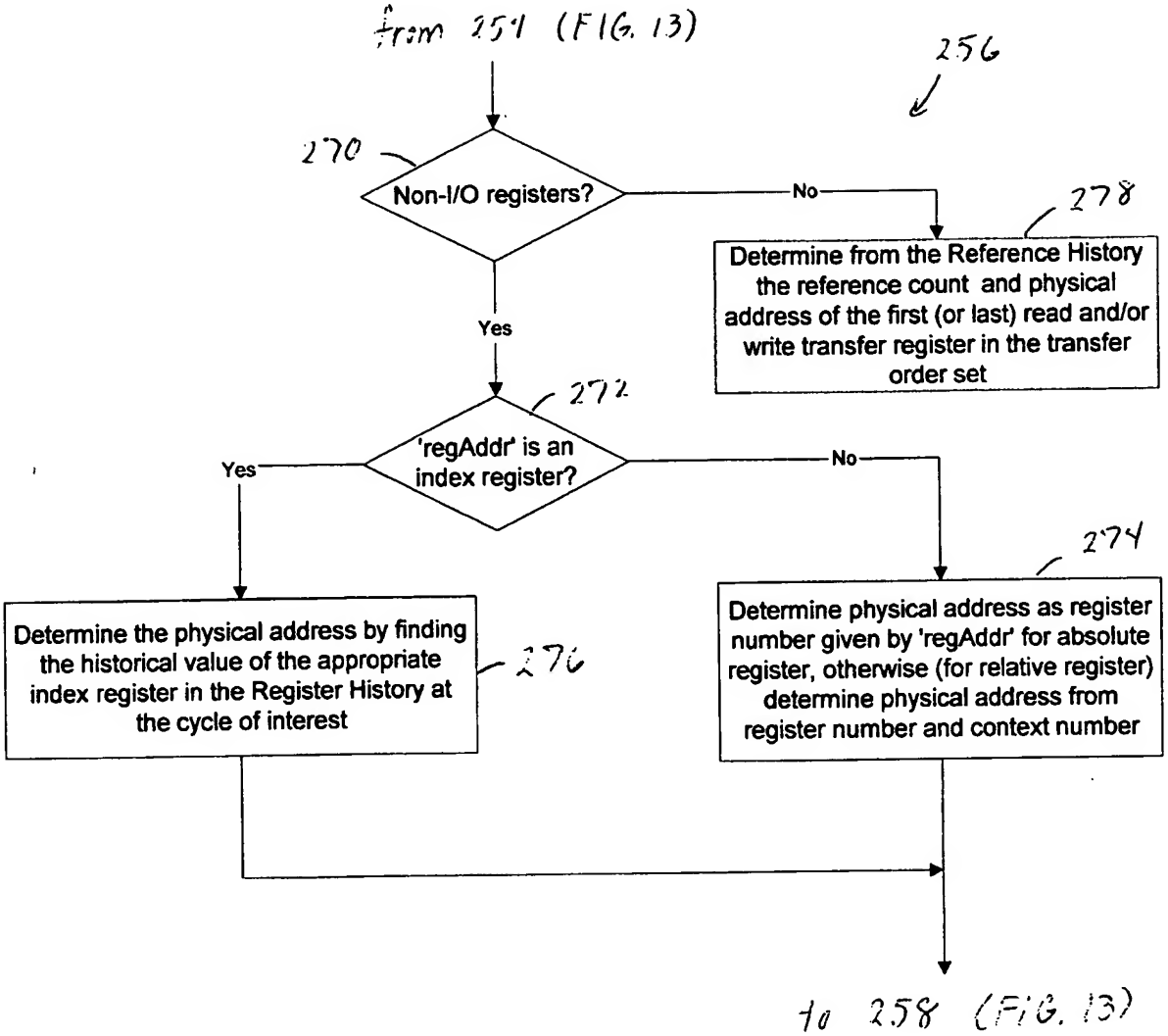
from 254 (FIG. 13)
256
270
Non-I/O registers?
No
278
Determine from the Reference History the reference count and physical address of the first (or last) read and/or write transfer register in the transfer order set
Yes
272
'regAddr' is an index register?
Yes
No
274
Determine the physical address by finding the historical value of the appropriate index register in the Register History at the cycle of interest
276
Determine physical address as register number given by 'regAddr' for absolute register, otherwise (for relative register) determine physical address from register number and context number
to 258 (FIG. 13)

FIG. 14

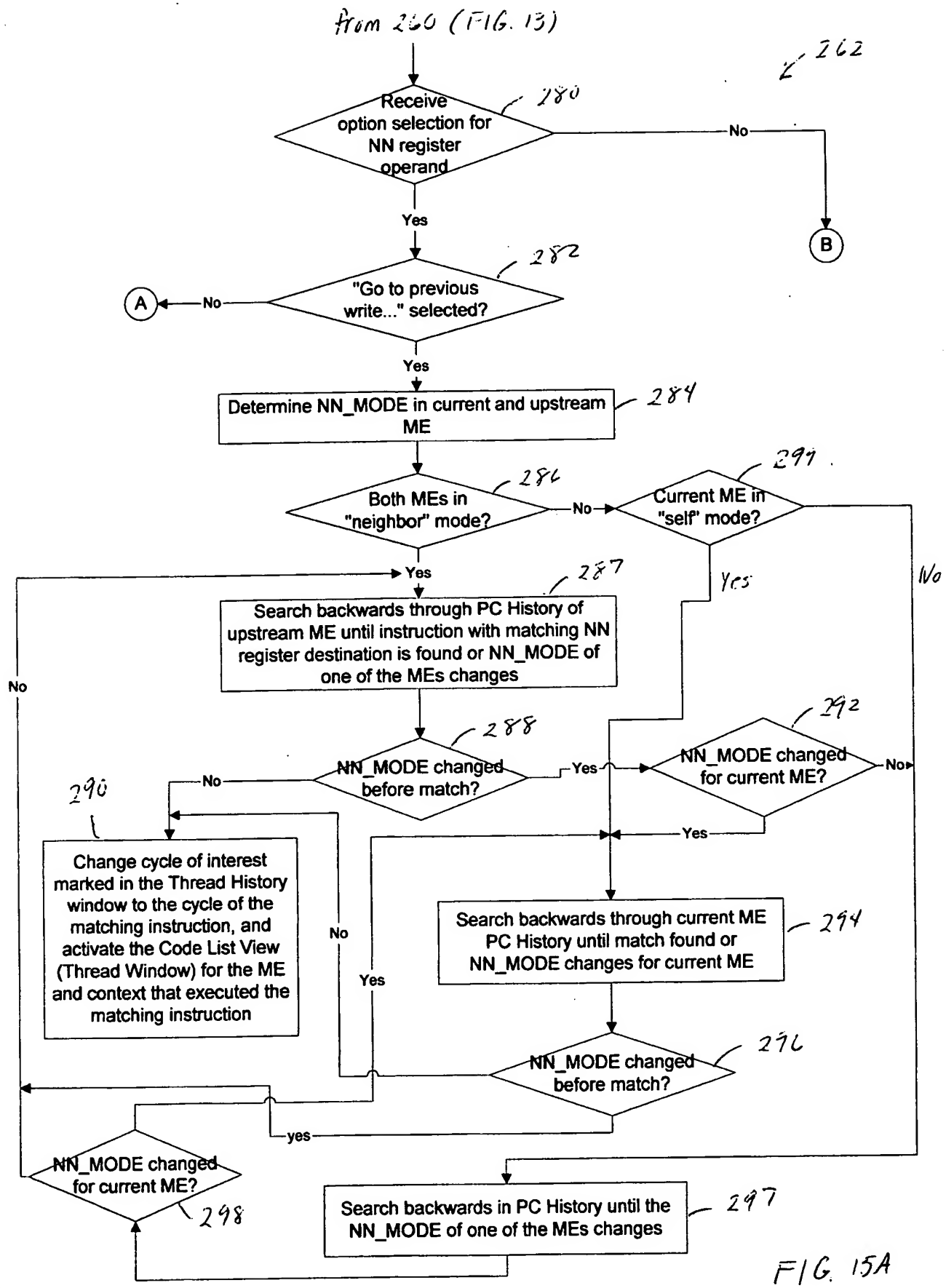
from 260 (FIG. 13)
262
Receive option selection for NN register operand
280
No
Yes
B
"Go to previous write..." selected?
282
No
A
Yes
Determine NN_MODE in current and upstream ME
284
Both MEs in "neighbor" mode?
286
No
Current ME in "self" mode?
299
Yes
No
Yes
Search backwards through PC History of upstream ME until instruction with matching NN register destination is found or NN_MODE of one of the MEs changes
287
No
NN_MODE changed before match?
288
No
Yes
NN_MODE changed for current ME?
292
No
Yes
290
Change cycle of interest marked in the Thread History window to the cycle of the matching instruction, and activate the Code List View (Thread Window) for the ME and context that executed the matching instruction
No
Yes
Search backwards through current ME PC History until match found or NN_MODE changes for current ME
294
NN_MODE changed before match?
296
yes
NN_MODE changed for current ME?
298
Search backwards in PC History until the NN_MODE of one of the MEs changes
297

FIG. 15A

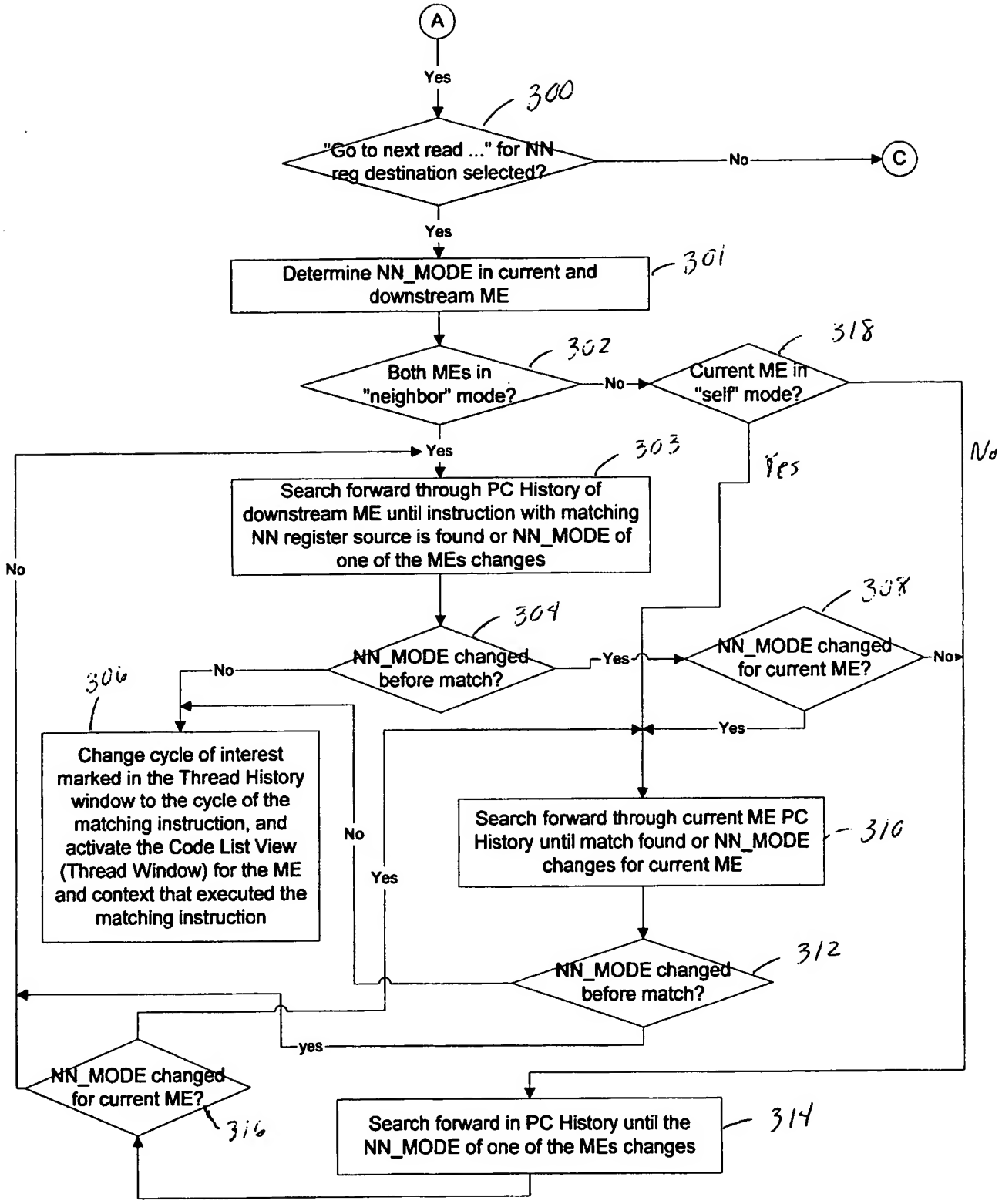
A
Yes
300
"Go to next read ..." for NN reg destination selected?
No
C
Yes
Determine NN_MODE in current and downstream ME
301
Both MEs in "neighbor" mode?
302
No
Current ME in "self" mode?
318
Yes
No
Yes
303
Search forward through PC History of downstream ME until instruction with matching NN register source is found or NN_MODE of one of the MEs changes
No
304
NN_MODE changed before match?
No
Yes
308
NN_MODE changed for current ME?
No
306
Yes
Change cycle of interest marked in the Thread History window to the cycle of the matching instruction, and activate the Code List View (Thread Window) for the ME and context that executed the matching instruction
No
Yes
Search forward through current ME PC History until match found or NN_MODE changes for current ME
310
NN_MODE changed before match?
312
yes
NN_MODE changed for current ME?
316
Search forward in PC History until the NN_MODE of one of the MEs changes
314

FIG. 15B

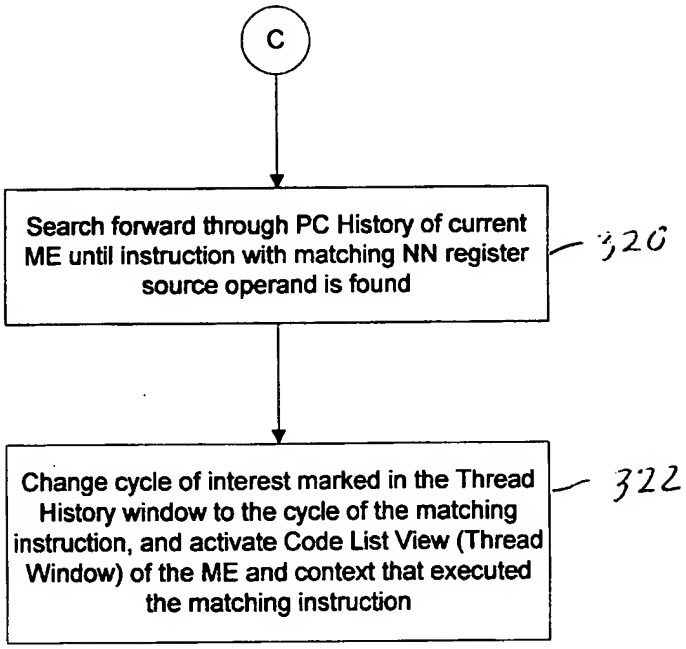
C
Search forward through PC History of current ME until instruction with matching NN register source operand is found
320
Change cycle of interest marked in the Thread History window to the cycle of the matching instruction, and activate Code List View (Thread Window) of the ME and context that executed the matching instruction
322

FIG. 15C

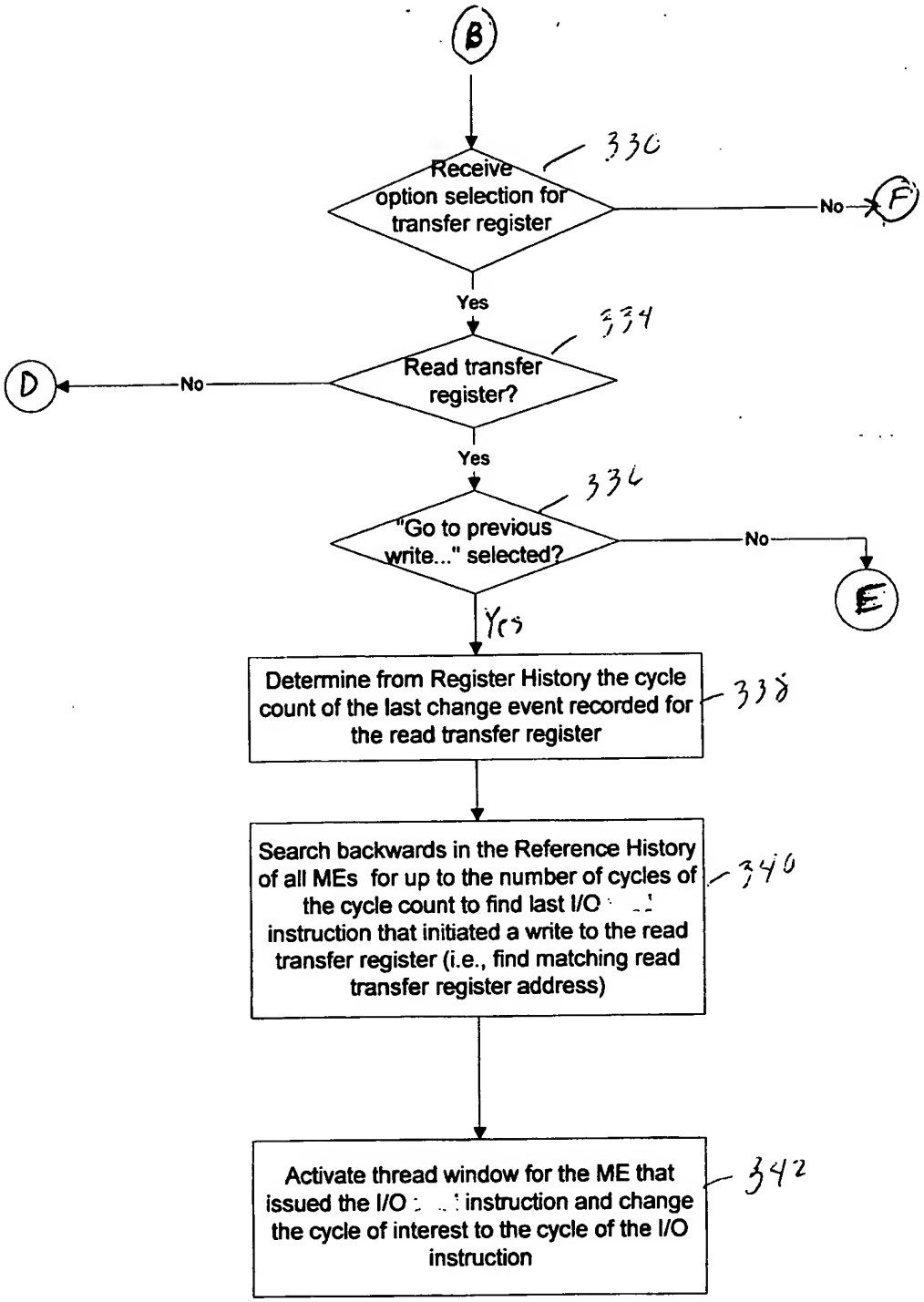
B
330
Receive option selection for transfer register
No
F
Yes
334
Read transfer register?
No
D
Yes
336
"Go to previous write..." selected?
No
E
Yes
Determine from Register History the cycle count of the last change event recorded for the read transfer register
338
Search backwards in the Reference History of all MEs for up to the number of cycles of the cycle count to find last I/O instruction that initiated a write to the read transfer register (i.e., find matching read transfer register address)
340
Activate thread window for the ME that issued the I/O instruction and change the cycle of interest to the cycle of the I/O instruction
342

FIG. 15D

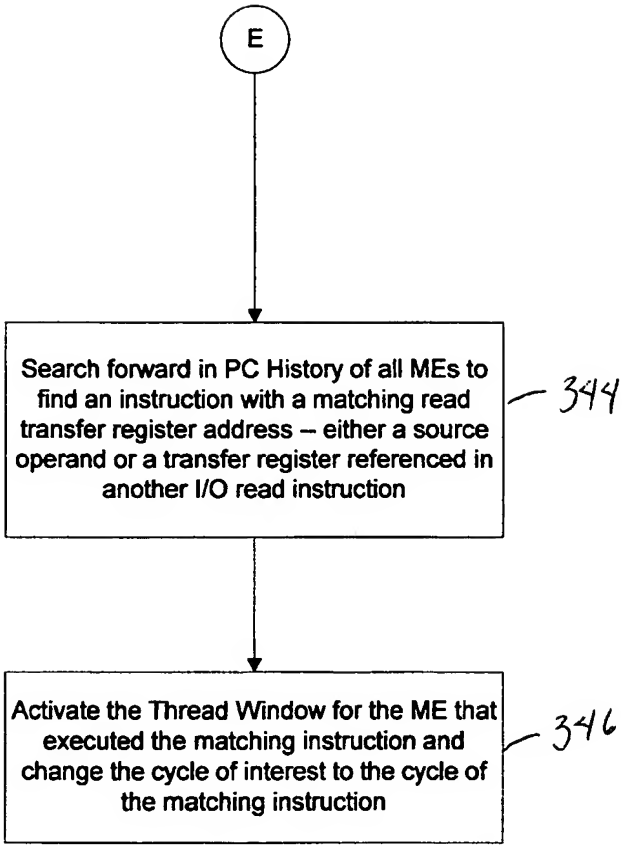
E
Search forward in PC History of all MEs to find an instruction with a matching read transfer register address – either a source operand or a transfer register referenced in another I/O read instruction
344
Activate the Thread Window for the ME that executed the matching instruction and change the cycle of interest to the cycle of the matching instruction
346

FIG. 15E

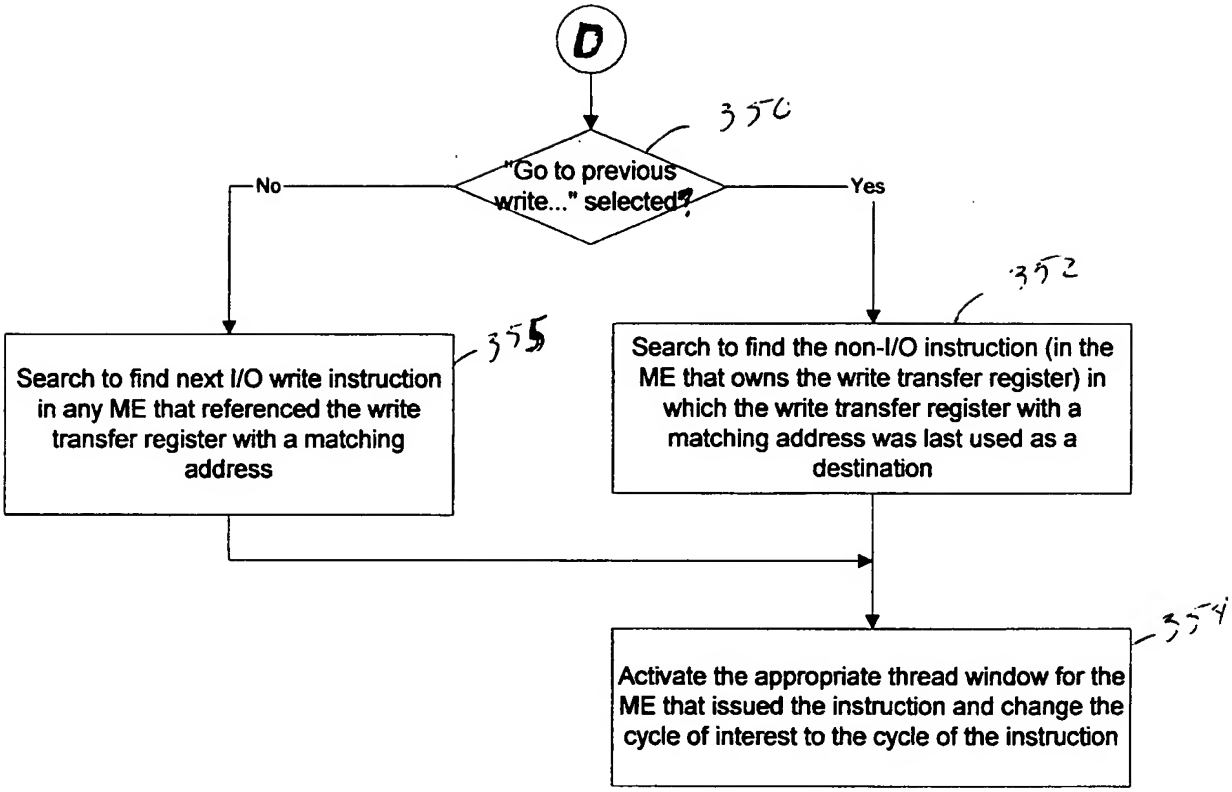
D
350
"Go to previous write..." selected?
No
Yes
352
Search to find the non-I/O instruction (in the ME that owns the write transfer register) in which the write transfer register with a matching address was last used as a destination
355
Search to find next I/O write instruction in any ME that referenced the write transfer register with a matching address
354
Activate the appropriate thread window for the ME that issued the instruction and change the cycle of interest to the cycle of the instruction

FIG. 15F

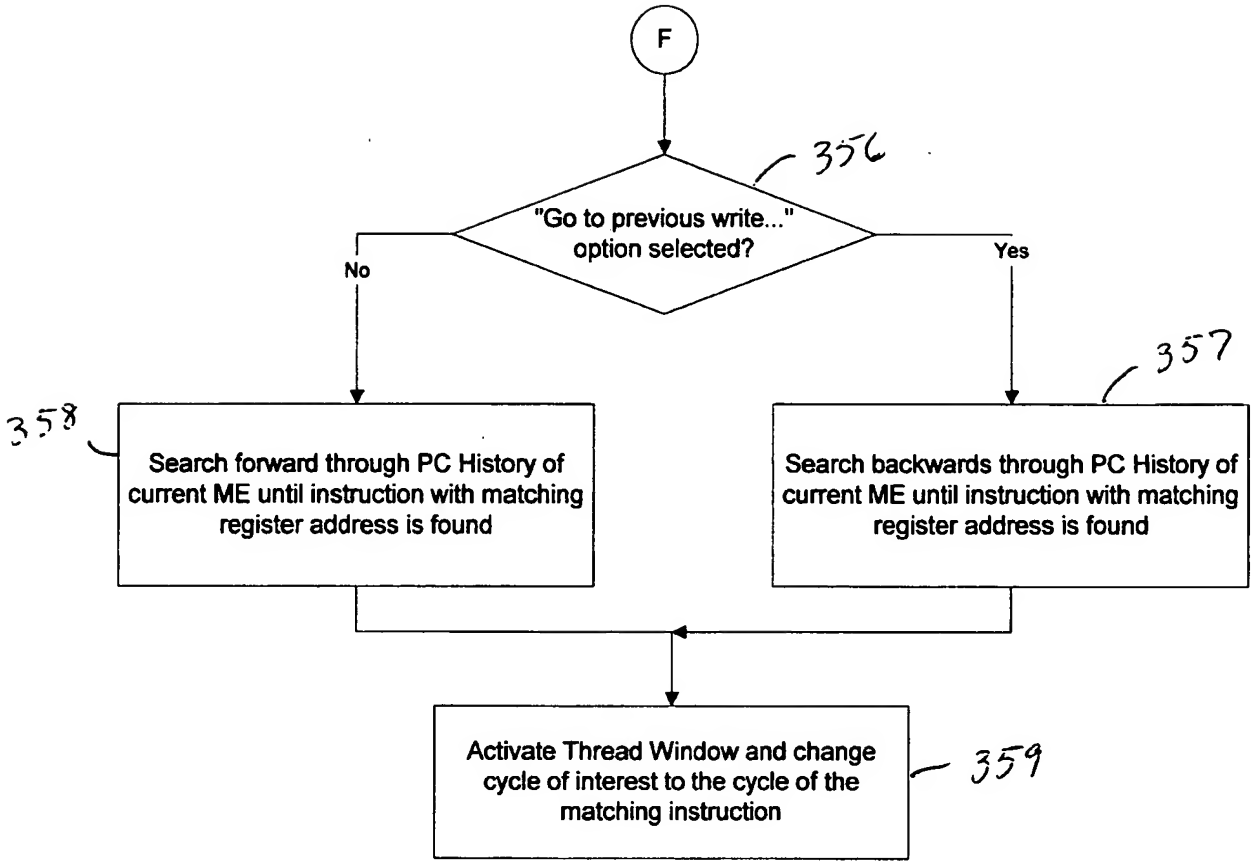
F
356
"Go to previous write..." option selected?
No
Yes
357
358
Search forward through PC History of current ME until instruction with matching register address is found
Search backwards through PC History of current ME until instruction with matching register address is found
Activate Thread Window and change cycle of interest to the cycle of the matching instruction
359

FIG. 15G

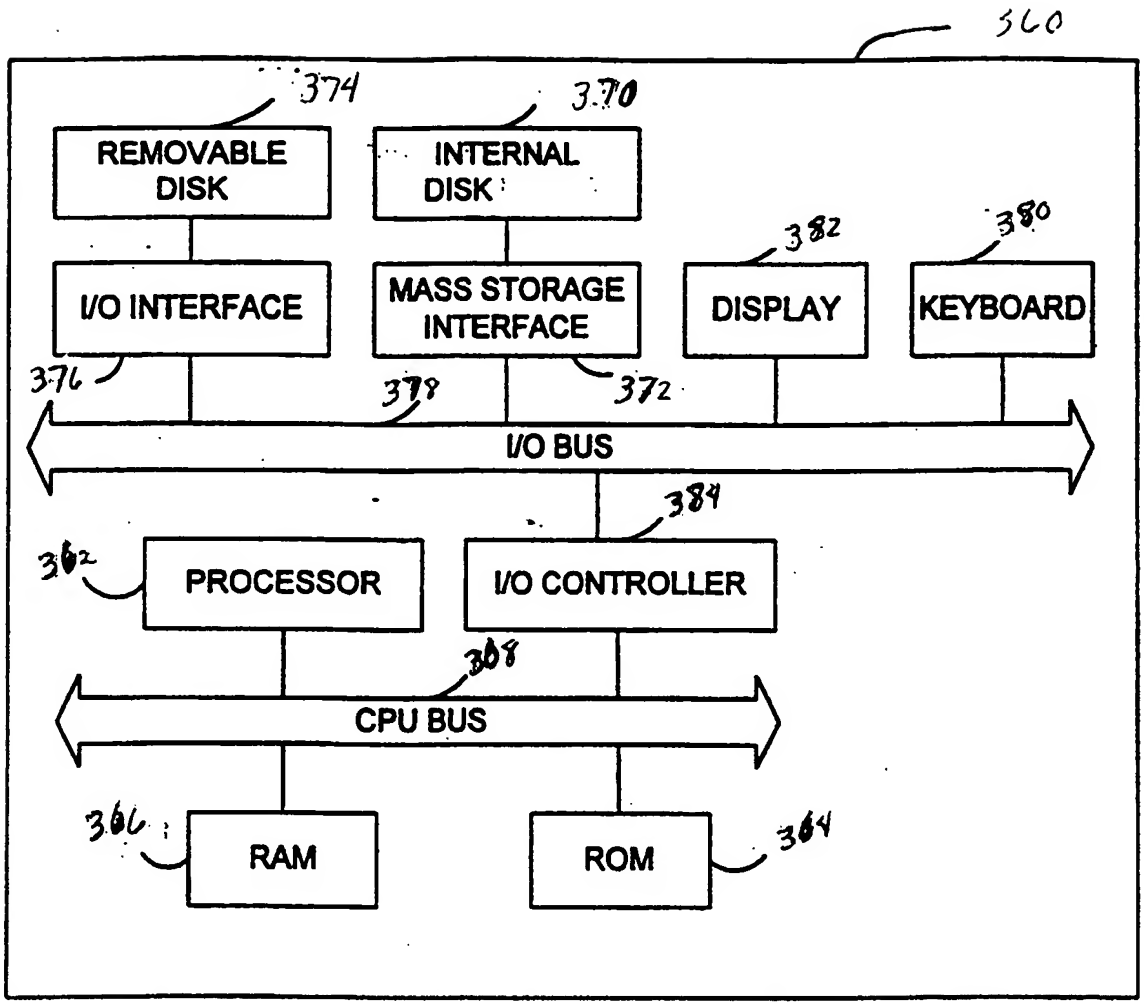
360
374
370
REMOVABLE DISK
INTERNAL DISK
382
380
I/O INTERFACE
MASS STORAGE INTERFACE
DISPLAY
KEYBOARD
376
378
372
I/O BUS
384
362
PROCESSOR
I/O CONTROLLER
368
CPU BUS
366
RAM
ROM
364

FIG. 16